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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	SUN-P4935
First Inventor or Application Identifier	Peter C. Damron
Title	Method and System for Translation...
Express Mail Label No.	EL575422730US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [ ] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original and a duplicate for fee processing)

2. [X] Specification [Total Pages 18]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 3]

4. Oath or Declaration [Total Pages 4]
a. [X] Newly executed (original or copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

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5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

jc886 U.S. PTO 09/629005 07/31/00

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
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[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____
Prior application information: Examiner _____ Group / Art Unit: _____
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label [redacted] (Insert Customer No. or Attach bar code label here) or [ ] Correspondence address below

Name	David B. Ritchie D'Alessandro & Ritchie				
Address	P. O. Box 640640				
City	San Jose	State	CA	Zip Code	95164-0640
Country	USA	Telephone	408-441-1100	Fax	408-441-8400

Name (Print/Type)	David B. Ritchie	Registration No. (Attorney/Agent)	31,562
Signature	[signature]	Date	7-31-2000

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08-02-00

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SUN-P4935

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Art Unit:
	)
Peter C. Damron	) Examiner:
	)
Serial No. [Not yet assigned]	)
	)
Filed: July 31, 2000	)
	)
For: METHOD AND SYSTEM FOR TRANSLATION LOOKASIDE BUFFER COHERENCE IN MULTI-PROCESSOR SYSTEMS	)

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Date of Deposit: July 31, 2000
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Diane Morse

Diane Morse

TRANSMITTAL LETTER

Honorable Assistant Commissioner
for Patents
Box Patent Application
Washington, D.C. 20231

Dear Sir:

Enclosed for filing please find the patent application for an invention entitled, "METHOD AND SYSTEM FOR TRANSLATION LOOKASIDE BUFFER COHERNCE IN MULTI-PROCESSOR SYSTEMS", filed on behalf of Sun Microsystems, Inc., assignee from inventor Peter C. Damron, including Utility Patent

Application Transmittal, 12 pages of specification, 5 pages of claims, 3 sheets of drawing figures, and 1 pages of Abstract. Also enclosed herewith are the Declaration, Power of Attorney.

The attorney's Docket Number is SUN-P4935.

Kindly address all communications regarding this application to:

David B. Ritchie
D'Alessandro & Ritchie
P.O. Box 640640
San Jose, CA 95164-0640
Telephone (408) 441-1100

A check in the amount of $768.00 is enclosed for the filing fee for a large entity, calculated as follows:

Basic Filing Fee:	$ 690.00
1 Additional Independent Claim:	$ 78.00
3 Additional Dependent Claims:	$ .00
Total Filing Fee:	$ 768.00

In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, the Assistant Commissioner is

hereby authorized to charge or credit the difference to our Deposit Account No. 04-0025.

A duplicate of this page is enclosed.

Respectfully submitted,
D'ALESSANDRO & RITCHIE

Dated: July 31, 2000

David B. Ritchie
Reg. No. 31,562

D'Alessandro & Ritchie
P.O. Box 640640
San Jose, CA 95164-0640
(408) 441-1100

hereby authorized to charge or credit the difference to our Deposit Account No. 04-0025.

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Respectfully submitted,
D'ALESSANDRO & RITCHIE

Dated: July 31, 2000

David B. Ritchie
Reg. No. 31,562

D'Alessandro & Ritchie
P.O. Box 640640
San Jose, CA 95164-0640
(408) 441-1100

This patent application is submitted in the name of inventor Peter C. Damron, a citizen of United States, assignor to Sun Microsystems, Inc., a Delaware Corporation.

SPECIFICATION

TITLE OF THE INVENTION

METHOD AND SYSTEM FOR TRANSLATION LOOKASIDE BUFFER COHERENCE IN MULTI-PROCESSOR SYSTEMS

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an apparatus, method and system for translation lookaside buffer ("TLB") coherence in computer systems; more particularly, this invention relates to an apparatus, method and system for TLB coherence in multi-processor computer systems.

The Related Art

Virtual memory systems allow the addressing of large amounts of memory as though all of that memory were the main memory of the computer system even though actual main memory may consist of a substantially lessor amount of storage space. Virtual memory systems accomplish this by providing memory management units which translate virtual memory addresses into physical memory addresses. The physical addresses may be stored in the main computer memory, in cache memory systems, or otherwise.

If the physical address is kept in the main computer memory, the main computer memory uses lookup tables to locate the physical address. The computer compares the virtual address to the values stored in the tables to determine the physical address. There are often several levels of tables, and the comparison takes a long time to locate. To overcome this delay, the physical address may be stored in cache memories. Cache memories are fast components to store recently

used data and instructions. The caches are first looked at by a processor before going to main memory for any information and are therefore usually connected so that they are rapidly accessible to the processors.

However, the cache memories must be addressed to obtain the information they contain. If addressed using physical addresses, then address translation is required from the virtual address to the physical address. To accomplish this without the use of lookup tables, a typical memory management unit uses a TLB to cache virtual page addresses that have been recently accessed along with their related physical page addresses.

When the TLB is provided with a virtual address that it has, it will provide the corresponding physical address. The physical address, if in the cache memory, allows for immediate access to information that is available to the processor without having to access the page lookup tables in the main memory. If the virtual address is not located in the TLB, otherwise known as a "TLB Miss," the physical address must be retrieved from the lookup tables in the main computer memory system. When the physical address is recovered, it is then stored along with other virtual addresses in the TLB so that it will be immediately accessible the next time. When the information is recovered, it is then stored in the cache under the physical address for immediate access.

Without the TLB, each memory access, either read or write, involved the main computer memory system. Typically the main computer memory system was distantly located, and also was relatively slow in operation. It wa ound that storing and mapping the addresses in a TLB would be more efficient since it was r to the processor and faster and reading and writing the data than the main computer mem y system. In a multiple processor system that has a TLB associated with each processor, each T B may contain data associated with a main computer

memory system, and each processor may process the data for the addresses and store the results in its respective TLB. Thus, it is possible that many different data values will exist among the multiple TLBs for a single address. This possible inconsistency among corresponding address locations is referred to in the art as the TLB coherency problem.

For a computer system with one processor, the time to provide TLB coherence is not time consuming. The operating system manages TLB coherence to both reference the physical address and/or to remove mappings entered to all the TLBs. However, it is time consuming to provide TLB coherence in multi-processor computer systems. Currently, the operating system sends messages to each individual processor. Each processor is then required to take a trap to the operating system to remove or enter the data into its respective TLB.

There are several disadvantages to the current TLB coherence method. First, it is expensive to provide a trap for each individual processor. Second, the process is very time consuming and slow. Lastly, the process disrupts the executing process of the system and results in future delay. Thus, there exists a need for a more efficient and quicker TLB coherence method for multi-processor systems.

SUMMARY OF THE INVENTION

This invention provides for a more efficient and cost effective way to obtain TLB coherence in computer systems. More specifically, this invention provides a more efficient and cost effective way to obtain TLB coherence in multi-processing computer systems.

A first embodiment of this invention is a method for maintaining TLB coherency in a computer system having a plurality of processors, each having an associated TLB for storing address translation data. The computer system accesses a virtual address in a TLB, locates a corresponding associated physical address, and sends a TLB message from the processor to the main communication network if: (1) the corresponding physical address was not located in the TLB and was required to be inputted into the TLB; (2) the corresponding physical address was removed from the TLB; or (3) the corresponding physical address was moved to another part of the computer network system. The main communication network then sends the TLB message to the plurality of processors.

Another embodiment of this invention is an apparatus for maintaining TLB coherency in a computer system having a plurality of processors, each having an associated TLB for storing address translation data, and the computer system having a plurality of independent paths upon which the plurality of processors are distributed. A TLB message generator having an accessed data address and a TLB message transmitted on said plurality of independent paths.

A further embodiment of this invention is a system for maintaining TLB coherency in a computer system having a plurality of processors, each having an associated TLB for storing address translation data, and the computer system having a plurality of independent paths upon which the plurality of processors are distributed among. The computer system performs an access to a data address from its associated TLB and a TLB message generator transmits a TLB

message to a main communication network. The main communication network then sends the TLB message to the plurality of processors.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this Specification, illustrate one or more embodiments of the invention and, together with the present description, serve to explain the principles of the invention.

In the drawings:

Fig. 1 is a diagram of a computer system having multiple processors.

Fig. 2 is a flow chart of one embodiment of the present invention.

Fig. 3 is a flow chart of one embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

One embodiment of the present invention is described herein in the context of TLB coherence in computer systems. Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to an implementation of the present invention as illustrated in the accompanying drawings. The same reference numbers will be used throughout the drawings and the following description to refer to the same or like parts.

In the interest of clarity, not all the routine features of the implementations described herein are described. It will of course be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made to achieve a developers' specific goals, such as compliance with system and business related constraints, and that these goals will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

Referring to Fig. 1, a computer system 10 that has a plurality of processors 14a, 14b, 14c each of which are connected to its own TLB 16a, 16b, 16c. There are independent paths 18a, 18b, 18c to which each processor 14a, 14b, 14c is connected.

Whenever a processor 14a accesses its associated TLB 16a for address translation data 20a to locate a corresponding physical address 22a with a virtual address 24a, the TLB 14a may or may not be able to locate the corresponding physical address. Should a TLB Miss occur, the physical address may be retrieved from the lookup tables in the computer memory system 26 and

recorded in the TLB 16a for future reference. Once recorded, the TLB message generator 11a sends out a TLB message with the accessed data address on its independent path 18a to the main communication network 12 to inform other processors 14b, 14c of the new corresponding physical address. The main communication network is, for example, a high speed data bus, or the like. Should the corresponding physical address 22a be located in the TLB 16a, the processor 14a may either modify the corresponding physical address 22a or move the corresponding physical address 22a to another part of the computer system 10. Again, the TLB message generator 11a sends a TLB message with the accessed data address to the main communication network which then transmits the TLB message on the independent paths 18b, 18c to other processors 14b, 14c for comparison of the address translation data 20b, 20c in their associated TLB 16b, 16c. If the corresponding physical address 22a is matched with the virtual address 24a, nothing further occurs.

Each of the other processors 14b, 14c will access its associated TLB 16b, 16c for the address translation data 20b, 20c and compare it with the data address in the TLB message. If the original processor 14a inputted a new physical address into its TLB 16a, then the TLB message will be a read access message to allow the other TLBs 16b, 16c to input the new physical address into its address translation data 20b, 20c. If the original processor modified, invalidated, or removed the physical address to another part of the computer network 10, then the TLB message will be a write access message to allow the other TLBs 16b, 16c to modify, invalidate or remove the physical address.

Now referring to Fig. 2, this invention provides for a method of TLB coherence in computer systems. In computer systems with multiple processors each having its own associated TLB, each processor may process the data for addresses and store the results in its respective

TLB. Thus, it is possible that many different data values will exist among the multiple TLBs for a single address. The present invention therefore provides for a more efficient and less costly method to maintain TLB coherency within a computer system so that each address will have the same data value. A virtual address is accessed in a TLB to locate the corresponding physical address 30. A TLB message generator sends a TLB message to the communication network 40 if: (1) the corresponding physical address was not located in the TLB and was required to be inputted into the TLB 32; (2) the corresponding physical address was removed from the TLB 34; or (3) the corresponding physical address was moved to another part of the computer network system 36. If the physical address 22a matches the physical address 22b, 22c of one of the other processors 14b, 14c, then that address translation data 20b, 20c should be modified, removed, or marked as invalid. If the corresponding physical address is matched with the virtual address 38, nothing further occurs.

If the corresponding physical address was inputted into the TLB, then the TLB message is a read access request to the other processors to input the address translation data into its associated TLB 42. However, if the corresponding physical address was modified, moved or invalidated, then the TLB message is a write access request to modify, remove or invalidate the corresponding physical address 44.

The TLB message is sent from the main communication network to each processor in the computer system. Once the TLB message is received, the request is compared to the address translation data on the associated TLB to determine whether the request affects the address translation data stored in the associated TLB 48. Now referring to Fig. 3, should the address translation data be affected, the processor will look to whether the TLB message is a read access TLB message 60 or a write access TLB message 62.

If the TLB message is a read access message 60 and the physical address in the corresponding TLB cannot be located 66, then the TLB message is ignored 74. However, if the physical address is located in the corresponding TLB 64, then the new accessed data address in the TLB message is added to the corresponding TLB 72.

If the TLB message is a write access message 62 and the physical address in the corresponding TLB cannot be located 68, then the TLB message is ignored 76. However, if the physical address is located in the corresponding TLB 70, then the physical address is modified, invalidated or removed from the corresponding TLB 78.

Referring to Fig. 1 and Fig. 2, this invention further provides for a system of TLB coherence in a computer system 10. The computer system 10 may have a plurality of processors 14a, 14b, 14c, each of which has its own associated TLB 16a, 16b, 16c and distributed among a plurality of independent paths 18a, 18b, 18c. A virtual address 24a is accessed in a TLB 16a to locate the corresponding physical address 22a. A TLB generator sends a TLB message to the main communication system 40 if: (1) the corresponding physical address was not located in the TLB and was required to be inputted into the TLB 32; (2) the corresponding physical address was removed from the TLB 34; or (3) the corresponding physical address was moved to another part of the computer network system 36.

Should a TLB Miss occur, the physical address may be retrieved from the lookup tables in the computer memory system 26 and recorded in the TLB 16a for future reference. The main communication network 12 then sends the TLB message with the accessed data address on the independent paths 18b, 18c to inform other processors 14b, 14c of the new corresponding physical address. Should the corresponding physical address be located in the TLB, the processor 14a may either remove the corresponding physical address 22a or move the physical

address 22a to another part of the computer system 10. The TLB message generator will send a TLB message with the accessed data address to the main communication network which transmits it on the independent paths 18b, 18c to other processors 14b, 14c for comparison of the address translation data 20b, 20c in their associated TLB 16b, 16c. If the physical address 22a matches the physical address 22b, 22c of one of the other processors 14b, 14c, then that address translation data 20b, 20c should be modified, removed, or marked as invalid. If the corresponding physical address 22a is matched with the virtual address 24a, nothing further occurs.

Each processor 14b, 14c will access its associated TLB 16b, 16c for address translation data and compare it with the data address in the TLB message 48. Now referring to Fig. 3, should the address translation data be affected, the processor will look to whether the TLB message is a read access TLB message 60 or a write access TLB message 62.

If the TLB message is a read access message 60 and the physical address in the corresponding TLB cannot be located 66, then the TLB message is ignored 74. However, if the physical address is located in the corresponding TLB 64, then the new accessed data address in the TLB message is added to the corresponding TLB 72.

If the TLB message is a write access message 62 and the physical address in the corresponding TLB cannot be located 68, then the TLB message is ignored 76. However, if the physical address is located in the corresponding TLB 70, then the physical address is modified, invalidated or removed from the corresponding TLB 78.

While embodiments and applications of this invention has been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. Thus, what has been disclosed is merely illustrative of the present invention and other arrangements or methods can be implemented by the those skilled in the art without departing from the spirit and scope of the present invention.

CLAIMS

We claim:

1. A method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of said processors having an associated TLB for storing an address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in said associated TLB and locating a corresponding associated physical address;

sending a TLB message from one of said plurality of processors to said main communication network if: (1) inputting a first entry into said associated TLB when said corresponding associated physical address is not located; (2) moving a second entry within said corresponding associated physical address to another location within said computer system; or (3) removing said second entry; and

sending said TLB message from said main communication network to said plurality of processors.

2. The method of claim 1 wherein said TLB message further comprises:

a request for a read access to said first entry to add said address translation data into said associated TLB.

3. The method of claim 1 wherein said TLB message further comprises:

a request for a write access to said second entry and to invalidate all copies of said second entry in each of said associated TLB in said plurality of processors.

4. The method of claim 1 further comprising:

comparing said first entry with said address translation data in said associated TLB and informing said associated TLB if said first entry affects said address data stored therein.

5. The method of claim 4 further comprising adding said address translation data in said first entry into said associated TLB in each of said plurality of processors.

6. The method of claim 1 further comprising:

comparing said second entry with said address data in said associated TLB and informing said associated TLB if said second entry affects said address data stored therein.

7. The method of claim 6 further comprising invalidating said address translation data in said second entry in said associated TLB in each of said plurality of processors.

8. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for maintaining TLB coherency in a computer system including a plurality of processors each having an associated TLB for storing address data and a main central processing unit coupled to the plurality of processors, said method comprising:

accessing a virtual address in said associated TLB and locating a corresponding associated physical address;

sending a TLB message from one of said plurality of processors to said main communication network if: (1) inputting a first entry into said associated TLB when said corresponding associated physical address is not located; (2) moving a second entry within said corresponding associated physical address to another location within said computer system; or (3) removing said second entry; and

sending said TLB message from said main communication network to said plurality of processors.

9. An electronic data processing apparatus, comprising:

a plurality of processors;

a plurality of TLBs, each of said plurality of TLBs connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, said plurality of processors distributed among said plurality of independent paths with each said processor connecting to one of said plurality of independent paths; and

a TLB message generator having an accessed data address and a TLB message transmitted on said plurality of independent paths.

10. The apparatus of claim 9 wherein said TLB message further comprises:

a read access message if said accessed data address is inputted into said associated TLB.

11. The apparatus of claim 9 wherein said TLB message further comprises:

a write access message if said accessed data address invalidates said address translation data in said associated TLB.

12. A system for TLB coherency in a computer system, comprising:

a plurality of processors;

a plurality of TLB, each of said plurality of TLB is connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, said plurality of processors is distributed among said plurality of independent paths with each processor and its associated TLB connecting to one of said plurality of independent paths;

performing an access to a data address from its said associated TLB;

a TLB message generator having a TLB message; and

transmitting said TLB message and said access data to a main communication network.

13. The system of claim 12 further comprising transmitting said TLB message and said access data on said plurality of independent paths and comparing said accessed data address with an address translation data of the information stored in each of said plurality of TLB and said TLB message will inform each of said plurality of TLB if said access data address affects data stored therein.

14. The system of claim 12 further comprising adding said access data address into said associated TLB in each of said plurality of processors.

15. The system of claim 12 further comprising invalidating said address translation data in said associated TLB in each of said plurality of processors.

16. The system of claim 12 further comprising moving said address translation data in said associated TLB in each of said plurality of processors to another part of the computer system.

17. The system of claim 12 wherein the TLB message generator further comprises:

a read access message if said accessed data address is inputted into said associated TLB.

18. The system of claim 12 wherein the TLB message generator further comprises:

a write access message if said accessed data invalidates said address translation data in said associated TLB.

ABSTRACT

This invention is an apparatus, method, and system for translational lookaside buffer coherency in computer systems having a plurality of processors, each having an associated TLB for storing address translation data, and the computer system having a plurality of independent paths upon which the plurality of processors are distributed and a TLB message transmitted on said plurality of independent paths.

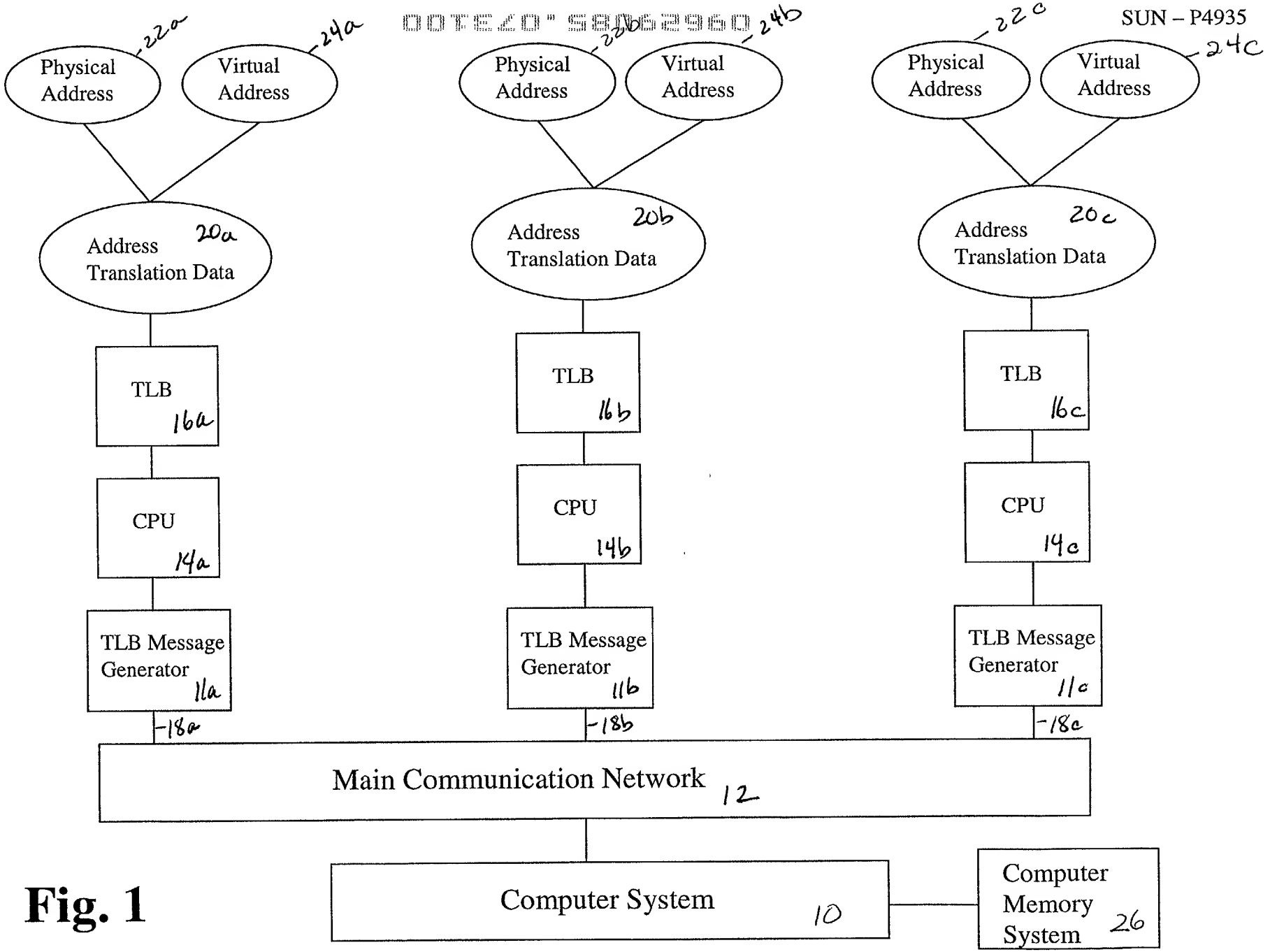

Fig. 1

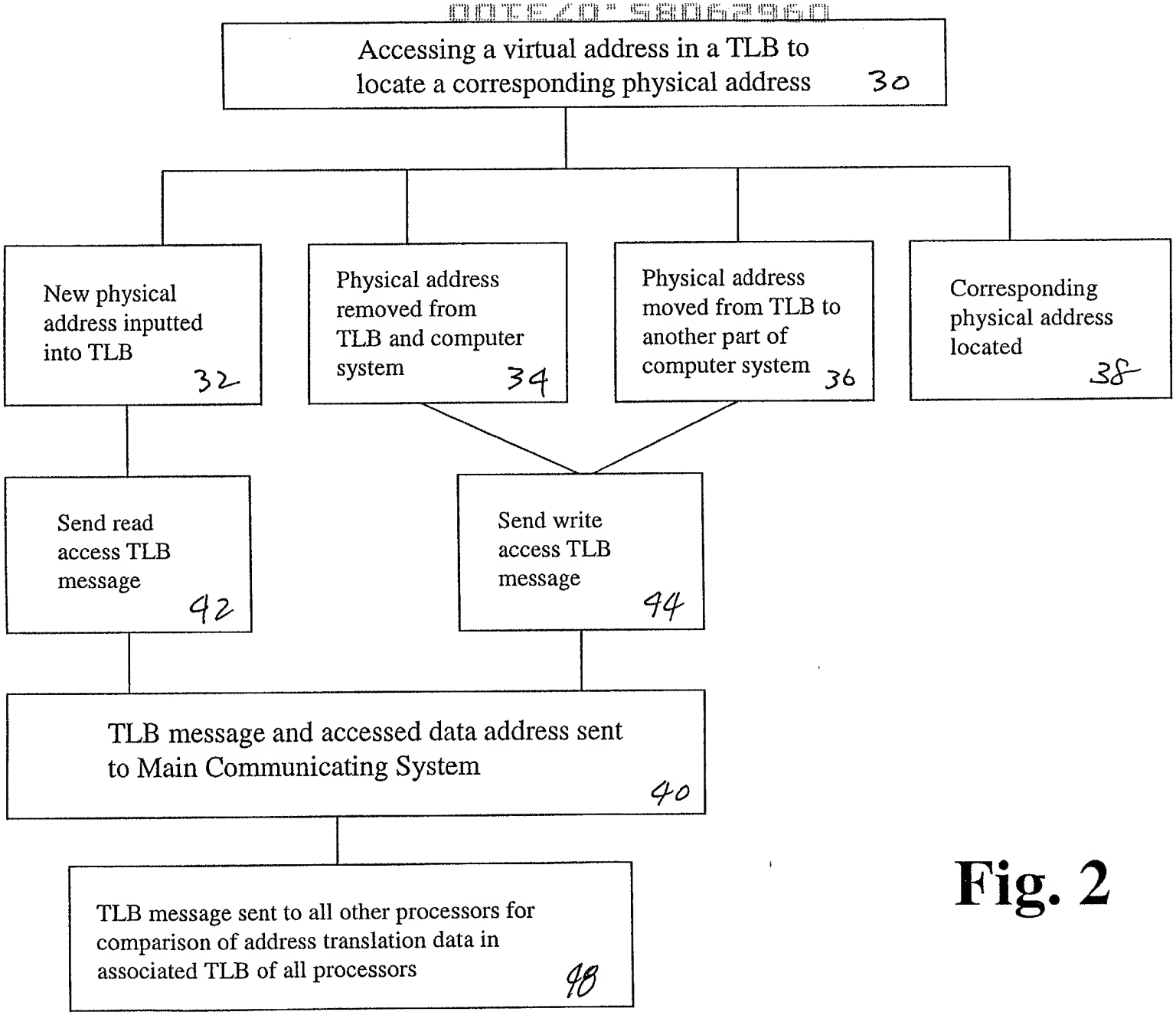

Fig. 2

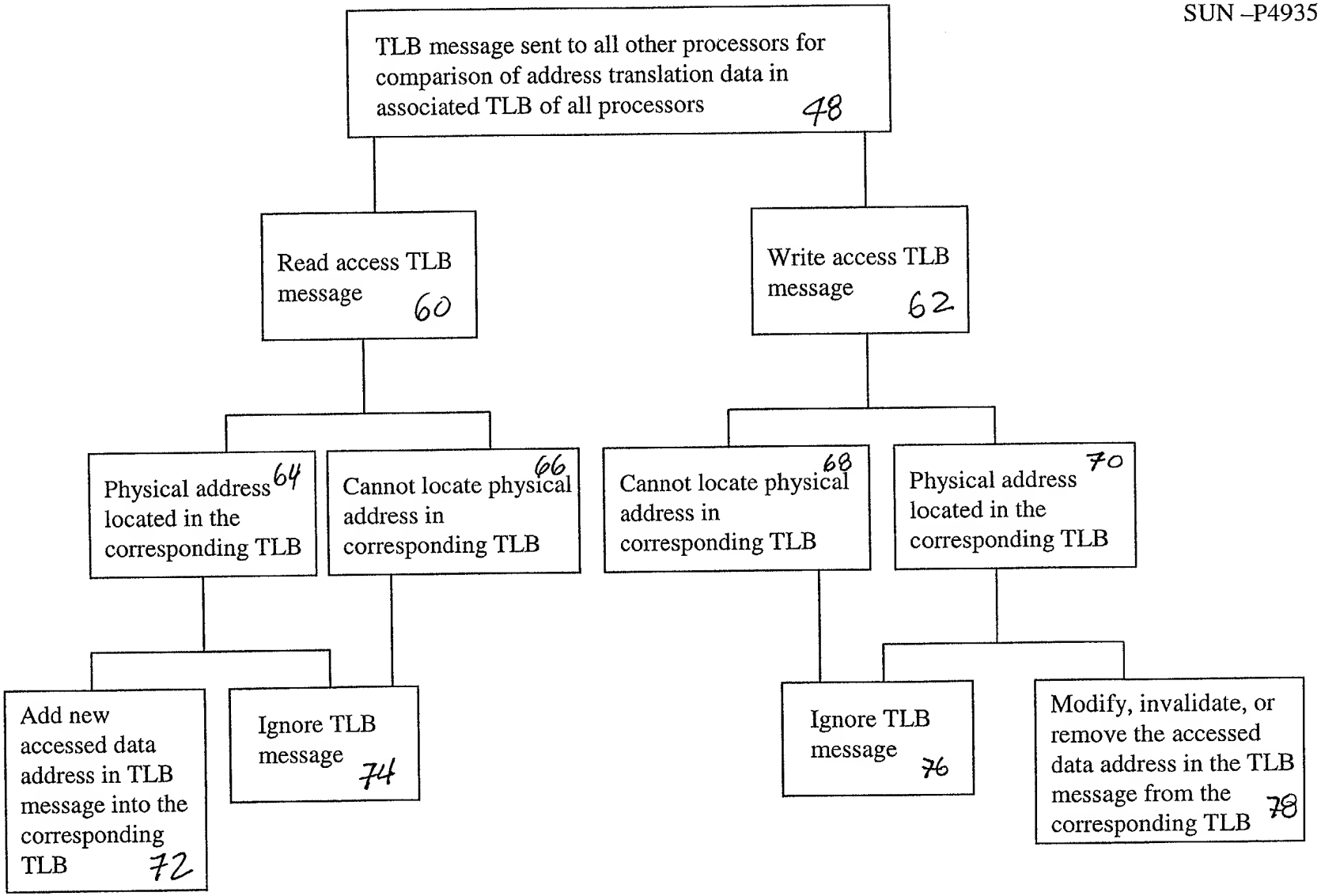
TLB message sent to all other processors for comparison of address translation data in associated TLB of all processors 48
Read access TLB message 60
Write access TLB message 62
Physical address located in the corresponding TLB 64
Cannot locate physical address in corresponding TLB 66
Cannot locate physical address in corresponding TLB 68
Physical address located in the corresponding TLB 70
Add new accessed data address in TLB message into the corresponding TLB 72
Ignore TLB message 74
Ignore TLB message 76
Modify, invalidate, or remove the accessed data address in the TLB message from the corresponding TLB 78

Fig. 3

DECLARATION & POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My correct residence, post office address and citizenship are stated below next to my name.

I believe myself to be the original, first and sole inventor (if only one name is listed below) or an original and first joint inventor (if more than one name is listed below) of the subject matter which is disclosed and claimed and for which a patent is sought on the invention entitled:

"Method and System for TLB Coherence on Multi-Processor Systems"

The specification of this subject matter:

X is attached hereto.

was filed on _____;

was assigned serial No. _____;

which was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified patent application, including the claims, as amended by any amendment(s) referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. §1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Month/Day/Year Filed	Yes	No
Number	Country	Month/Day/Year Filed	Yes	No
Number	Country	Month/Day/Year Filed	Yes	No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in these prior United States application(s) in the manner provided by 35 U.S.C. §112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

Application No.	Filing Date	Status (Issued, Pending, Abandoned)
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I hereby appoint Kenneth D'Alessandro, Registration No. 29,144; David B. Ritchie, Registration No. 31,562; Marc S. Hanish, Registration No. 42,626; John P. Schaub, Registration No. 42,125; Gerhard W. Thielman, Registration No. 43,186; Loren K. Thompson, Registration No. 45,918; Adrienne Yeung, Registration No. 44,000; Steven J. Robbins, Registration No. 40,299; Kenneth Olsen, Registration No. 26,493; Timothy J. Crean, Registration No. 37,116; Robert S. Hauser, Registration No. 37,847; Joseph T. FitzGerald, Registration No. 33,881; Alexander E. Silverman, Registration No. 37,940; Christine S. Lam, Registration No. 37,489; Anirma Rakshpal Gupta, Registration No. 38,275; Sean P. Lewis, Registration No. 42,798; Michael J. Schallop, Registration No. 44,319; Bernice B. Chen, Registration No. 42,403; Kenta Suzue, Registration No. 45,145; Noreen Krall, Registration No. 39,734; Richard J. Lutton, Jr., Registration No. 39,756; Monica Lee, Registration No. 40,696; Marc D. Foodman, Registration No. 34,110; and Naren Chaganti, Registration No. 44,602 as attorneys of record with full power of substitution and revocation, to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith.

Please send all correspondence and direct all telephone calls to:

D'Alessandro & Ritchie
P.O. Box 640640
San Jose, CA 95164-0640
Telephone (408) 441-1100

I, the undersigned, declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code,

and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

FULL NAME OF INVENTOR 1	FIRST Name	MIDDLE Initial(s)	LAST Name
	Peter	C.	Damron

RESIDENCE AND Citizenship	City	State or Foreign Country	Country of
CITIZENSHIP	Fremont	California	United States of America

POST OFFICE Code ADDRESS	Number and Street	City	State or Country	Zip
	4430 Romilly Way	Fremont	CA	94536

I further declare that all statements made herein of my own knowledge are true and that all statements made upon information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Peter C. Damron 7/25/00

Signature of Inventor 1 Date

37 C.F.R. §1.56
Duty to disclose information material to patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1,97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability
(2) It refutes, or is inconsistent with, a position the applicant takes in:
    (i) Opposing an argument of unpatentability relied on by the Office, or
    (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;
(2) Each attorney or agent who prepares or prosecutes the application; and
(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whon

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

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